# M220x Series

## 9x14 mm, 3.3/2.5/1.8 Volt, PECL/LVDS/CML, Clock Oscillator

- Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

**Applications:**

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

### Ordering Information

M220 0 6 8 B P J 00.0000 MHz

**Product Series**

**Supply Voltage**
**0:** 3.3 V **1:** 2.5 V
**2:** 1.8 V

**Temperature Range**
**2:** -40°C to +85°C (see note 1)
**6:** -20°C to +70°C

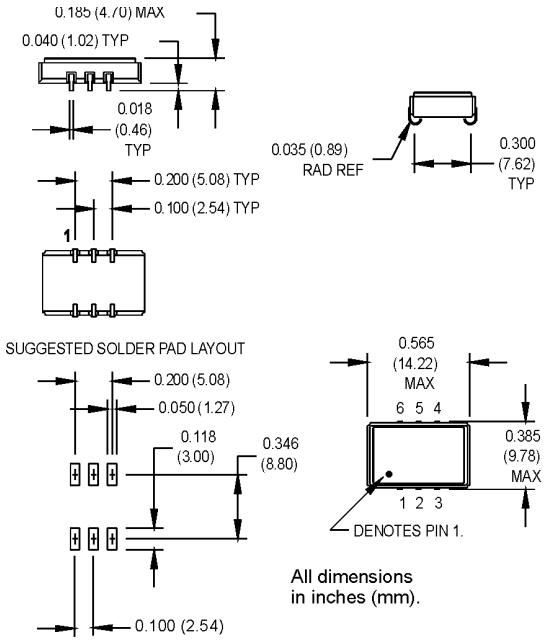
**Stability**
**4:** ±50 ppm **3:** ±100 ppm
**8:** ±20 ppm

**Enable/Disable**
**B:** Enable High (pin 1) **G:** Enable High (pin 2)
**S:** Enable Low (pin 1) **M:** Enable Low (pin 2)
**U:** No Enable/Disable

**Logic Type**
**P:** LVPECL **L:** LVDS
**M:** CML

**Package/Lead Configuration**
**J:** 9x14 mm J-lead

**Frequency (customer specified)**




All dimensions in inches (mm).

**PIN 1 ENABLE**
Pin1: Enable/Disable
Pin2: N/C
Pin3: Ground
Pin4: Output Q (LVPECL,LVDS,CML)
Pin5: Output $\bar{Q}$ (LVPECL,LVDS,CML)
Pin6: Vcc

**PIN 2 ENABLE**
Pin1: N/C
Pin2: Enable/Disable
Pin3: Ground
Pin4: Output Q (LVPECL,LVDS,CML)
Pin5: Output $\bar{Q}$ (LVPECL,LVDS,CML)
Pin6: Vcc

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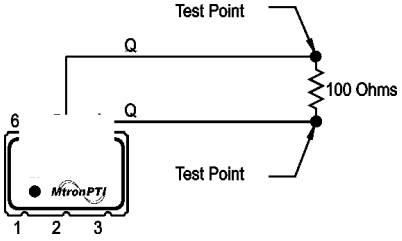
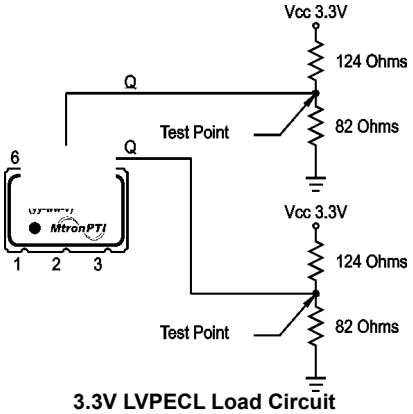
| | PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition/Notes |
|---|---|---|---|---|---|---|---|
| Electrical Specifications | Frequency Range | F | 150 | | 1400 | MHz | See Note 2 |
| | Operating Temperature | TA | (See ordering information) | | | | See Note 1 |
| | Storage Temperature | Ts | -55 | | +125 | °C | |
| | Frequency Stability | ΔF/F | (See ordering information) | | | | See Note 3 |
| | Aging | | | | | | |
| | 1st Year | | -3 | | +3 | ppm | |
| | Thereafter (per year) | | -1 | | +1 | ppm | |
| | Supply Voltage | Vcc | 1.71 | 1.8 | 1.89 | V | |
| | | | 2.375 | 2.5 | 2.625 | V | |
| | | | 3.135 | 3.3 | 3.465 | V | |
| | Input Current | Icc | | | 125 | mA | LVPECL/LVDS/CML |
| | Load | | 50 Ohms to (Vcc -2) Vdc<br>100 Ohm differential load | | | | See Note 4<br>LVPECL Waveform<br>LVDS/CML Waveform |
| | Symmetry (Duty Cycle) | | 45 | | 55 | % | @ 50% of waveform |
| | Output Skew | | | TBD | | | |
| | Differential Voltage | | 350 | 425<br>TBD | 500 | mVppd | LVDS<br>CML |
| | Common Mode Output Voltage | Vcm | | 1.2 | | V | LVDS |
| | Logic "1" Level | Voh | Vcc -1.02 | | | V | LVPECL |
| | Logic "0" Level | Vol | | | Vcc -1.63 | V | LVPECL |
| | Rise/Fall Time | Tr/Tf | | 0.23 | 0.50 | ns | @ 20/80% LVPECL |
| | Enable Function | | 80% Vcc min. or N/C: output active<br>20% Vcc max.: output disables to high-Z | | | | Output Option B or G |
| | | | 20% Vcc max: output active<br>80% Vcc min.: output disables to high-Z | | | | Output Option S or M |
| | Start up Time | | | 10 | | ms | |
| | Phase Jitter<br>@ 622.08 MHz | ϕJ | | 0.3 | | ps RMS | Integrated 12 kHz – 20 MHz |
| | Phase Noise<br>10 Hz<br>100 Hz<br>1 KHz<br>10 KHz<br>100 KHz<br>1 MHz<br>10 MHz<br>40 MHz | | | <br>-50<br>-80<br>-106<br>-117<br>-120<br>-130<br>-147<br>-150 | | | @ 622.08 MHz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| Environmental | Mechanical Shock | Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave) | | | | | |
| | Vibration | Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz) | | | | | |
| | Hermeticity | Per MIL-STD-202, Method 112, ($1x10^{-8}$ atm. cc/s of Helium) | | | | | |
| | Thermal Cycle | Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles) | | | | | |
| | Solderability | Per EIAJ-STD-002 | | | | | |
| | Soldering Conditions | +240°C max. for 10 secs. | | | | | |

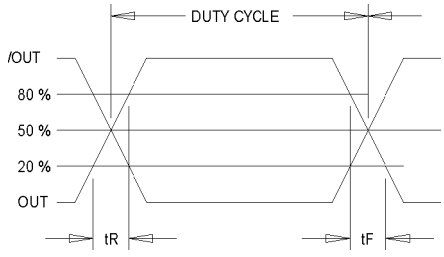
Note 1: If the device is powered up below -20°C and then the ambient temperature rises 105°C during normal operation, the output will be interrupted for approximately 2-3 ms. A correction is in process an will be available Q1 2007.
Note 2: Contact factory for exact frequency availability over 945 MHz
Note 3: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 4: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.




**LVDS Load Circuit**




**3.3V LVPECL Load Circuit**




**Output Waveform: LVDS/CML/PECL**